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(54) Arrangement for measuring a quiescent current of an integrated monolithic digital circuit, integrated monolithic digital circuit provided with such an arrangement and testing apparatus provided with such an arrangement.

(57) An arrangement is proposed for measuring a quiescent current of a digital IC. The arrangement comprises a current sensor in series with the IC and the supply, voltage stabilization means for stabilizing the voltage across the IC and signal processing means coupled thereto for processing the measured quiescent current. The quiescent current is measured when no flip-flops are switched in the IC. By means of the arrangement, there can be measured rapidly and accurately whether the quiescent current assumes an abnormal value, which indicates that the IC exhibits defects. The signal processing means comprise a current mirror, which is coupled to a current comparator circuit supplying a digital output signal for determining a defect.

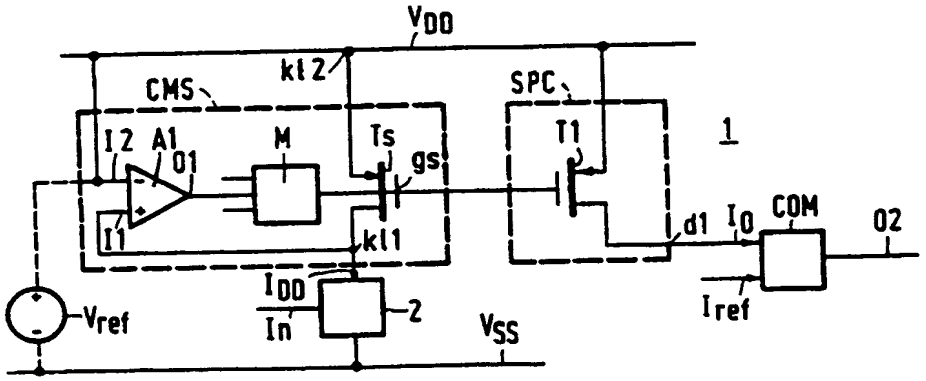

FIG.1A

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Arrangement for measuring a quiescent current of an integrated monolithic digital circuit, integrated monolithic digital circuit provided with such a arrangement and testing apparatus provided with such an arrangement.

The invention relates to an arrangement for measuring a quiescent current of an integrated monolithic digital circuit, which arrangement comprises a current sensor for measuring the quiescent current, which is provided with a first connection terminal for coupling to a supply terminal of the integrated monolithic circuit and with a second connection terminal for coupling to a supply.

The invention further relates to an integrated monolithic digital circuit provided with such an arrangement.

The invention moreover relates to a testing apparatus provided with such an arrangement.

Such an arrangement for measuring a quiescent current of an integrated monolithic digital circuit is known from the article "Built-In-Current Testing-Feasibility Study", W. Maly and P. Nigh, Proceeding ICCAD 1988, pp. 340-343, IEEE. In this publication, testing of digital VLSI circuits by means of a current sensor incorporated in the integrated monolithic circuit is described. As current sensor a sensor having a non-linear characteristic, more particularly a bipolar transistor as current sensor having an exponential I-U characteristic, is described. The current sensor is included between the monolithic circuit and the supply of the monolithic circuit and serves to measure abnormal quiescent currents, which are due, for example, to shortcircuits and/or floating gate electrodes of, for example, MOS-FET's in the VLSI circuit. There is measured dynamically, that is to say that test vectors are supplied at inputs of the VLSI circuit and the quiescent current is measured in rest periods between switching operations. If the VLSI circuit operates satisfactorily, the quiescent current can be orders of magnitude smaller as compared with an unsatisfactory operation. A quiescent current measurement can therefore give an indication about a satisfactory or an unsatisfactory operation of the VLSI circuit. The voltage across the current sensor is compared with a reference voltage in quiescent current periods. If the voltage is larger than a predetermined value, the VLSI circuit is very likely to be defective. Because of the exponential characteristic of the transistor, it is possible to discriminate between comparatively large current during switching of transistors in the VLSI circuit and the comparatively small quiescent currents. In the arrangement, a bipolar current sensor is used in a MOS environment, which may give rise to problems with respect to integration in the same integrated monolithic digital circuit. Further, a satisfactorily operating VLSI circuit, in which a current sensor is included, will operate more slowly than a VLSI circuit without a current sensor.

The invention has inter alia for its object to provide an arrangement of the kind mentioned in the opening paragraph, by means of which a rapid quiescent current measurement can be carried out with a high resolution.

An arrangement for measuring a quiescent current of an integrated monolithic digital circuit according to the invention is characterized in that the arrangement comprises voltage stabilization means for stabilizing a voltage at the first connection terminal and signal processing means coupled to the voltage stabilization means for signal processing of the quiescent current. Due to the fact that also with large current variations the voltage across the current sensor remains substantially equal, on the one hand a high resolution will be attained when measuring the quiescent current and on the other hand the operation of the integrated monolithic circuit will not be adversely affected with peak currents during switching.

An embodiment of an arrangement according to the invention is characterized in that the voltage stabilization means comprise a differential amplifier, of which a first input is coupled to the first connection terminal, a second input is coupled to the second connection terminal or to a connection terminal for connection to a reference voltage source and an output is coupled to a gate electrode of the transistor. In the case in which the second input is coupled to the second connection terminal, with a predetermined offset voltage (for example 100 mV) of the differential amplifier it will be achieved that the voltage drop across the transistor is low and because of the feedback loop the voltage drop will vary only comparatively slightly even with comparatively large current variations. In the case in which the second input is coupled to a connection terminal for connection to a reference voltage source, for integrated monolithic circuits to which a higher external supply voltage is supplied then an internal supply voltage as operating voltage ("voltage down conversion"), functions of current measurement, voltage stabilization and stepping down of the external supply voltage will be combined. If the predetermined offset voltage is substantially O V, the voltage at the first connection terminal and hence the operating voltag of the integrated monolithic circuit will be substantially equal to the voltage of th reference voltage source.

An embodiment of an arrangement according

to the invention is characterized in that the output of the differential amplifier is coupled to the gate electrode via a modification circuit for modifying the operation of the current sensor outside a quiescent current measurement period or outside a quiescent current measurement of the integrated monolithic circuit. As a result, in normal conditions an operation can be attained which is substantially equal to an operation without a current sensor in case the arrangement is integrated with the integrated monolithic circuit.

An embodiment of an arrangement according to the invention is characterized in that the signal processing means comprise a first transistor, which constitutes with the current sensor a current mirror configuration, which is designed to supply via an output electrode of the transistor a current which is a mirror image of the quiescent current. As a result, a measured quiescent current is obtained, on which further operations can be carried out without the operation of the integrated monolithic circuit being substantially adversely affected, which could be the case, for example, if an ohmic load should be coupled to the first connection terminal for obtaining a measuring voltage derived from the quiescent current.

A further embodiment of an arrangement according to the invention is characterized in that the signal processing means comprise a differential amplifier, which is coupled via a first input of the first connection terminal, via a second input to the output electrode of the first transistor and via an output to a gate electrode of a second transistor, which second transistor is coupled via a first output electrode to the output electrode of the first transistor, while a second output electrode of the second transistor serves to supply a further processed quiescent current. The differential amplifier of the voltage stabilization means is adjusted so that the voltage drop across the current sensor is very low. The supply voltage of the integrated monolithic circuit is then very stable and substantially equal to the external supply voltage. The differential amplifier of the signal processing means and the second transistor ensure that the first transistor, like the current sensor transistor, operates in the linear range (triode range). As a result, it is achieved that a current equal (with equal geometric dimensions of the current sensor transistor and the first transistor) or a current proportional (with different geometric dimensions) to that flowing through the current sensor transistor flows through the first transistor. The second transistor suppli s a measured current for further processing.

An embodiment of an arrangement according to the invention is characterized in that the signal processing means further comprise transistors, which constitute with th current sensor a current mirror configuration, while for obtaining different processed quiescent currents the transistors of the signal processing means have different geometric dimensions. As a result, different currents proportional to the quiescent current are obtained for further processing.

An integrated monolithic digital circuit according to the invention, which comprises at least one subcircuit, is characterized in that the integrated monolithic circuit comprises at least one arrangement or at least a part thereof as claimed in any one of Claims 1 to 10 for measuring the quiescent current of subcircuits, of combinations of subcircuits, or of all subcircuits. If the integrated monolithic circuit comprises the current sensor, the voltage stabilization means and the signal processing means, the measured quiescent current can be passed to a connection pin of the integrated monolithic circuit for further processing at the printed circuit board level or by means of a testing apparatus for integrated monolithic digital circuits. If the comparison means are also integrated on the integrated monolithic circuit (everything "on-chip"), before a next switching peak the digitized value of the processed quiescent current may be introduced, for example, into a flip-flop. For an integrated monolithic circuit comprising several subcircuits, the digitized values of the quiescent currents obtained can be further processed in "on-chip" or "off-chip" testing apparatuses, which used, for example, techniques, such as "scan-test", "self-test" and "boundary scan". With respect to the last-mentioned techniques, reference may be made to the relevant literature.

The invention will be described more fully with reference to a drawing, in which:

Fig. 1A is a diagrammatic representation of an arrangement according to the invention,

Fig. 1B shows a current through an integrated monolithic digital circuit as a function of time when supplying a given test vector at inputs thereof,

Fig. 2 shows an embodiment of signal processing means and comparison means in an arrangement according to the invention,

Fig. 3 shows an embodiment of multiplication of a measured quiescent current,

Fig. 4A shows a current measurement according to the invention to measure a metastable condition in a digital circuit,

Fig. 4B shows a current of such a circuit,

Fig. 4C shows a voltage at an output terminal of such a digital circuit,

Fig. 5 shows a current measurement according to the invention to obtain information about stability of outputs of combinatorial digital subcircuits,

Fig. 6 shows a testing apparatus provided

with an arrangement according to the invention.

Fig. 7A shows an embodiment of the current measuring circuit with an embodiment of the modification circuit,

Fig. 7B shows another embodiment of the modification circuit,

Figs. 8A and 8B show configurations of IC's including a current measuring arrangement according to the invention,

Fig. 9 shows the coupling of the current measuring arrangement with a scan chain in an IC, and

Fig. 10 shows the coupling of the current measuring circuit according to the invention with a self-test circuit in an IC.

Fig. 1A shows diagrammatically an arrangement 1 according to the invention, which is coupled to an integrated monolithic digital circuit 2, of which a quiescent current I_{DD} is measured. The arrangem nt 1 comprises a transistor Ts as current sensor for measuring the quiescent current. The transistor Ts is connected in series with the integrated monolithic circuit 2 between a first supply line V_{DD} and a second supply line V_{SS}. According to the invention, the voltage at a first connection terminal kl1 is stabilized with the aid of voltage stabilization means, in the example shown with the aid of a fed-back differential amplifier A1. The current sensor Ts is connected via a second connection terminal kl2 to the supply line V_{DD}. The current sensor Ts and the differential amplifier A1 constitute a current measuring circuit CMS according to the invention. The differential amplifier A1 is connected through a first input I1(+) to the first connection terminal kl1, through a second input I2(-) to the supply line V_{DD} or through a reference source V_{ref} to the supply line V_{SS} and through an output 01 directly or via a modification circuit M to a gate electrode gs of the current sensor Ts. The modification circuit M may be an amplifier or a filter and may have additional inputs to render the transistor Ts completely conducting outside the measurement of the quiescent current. If the input I2 is connected to the supply line V_{DD}, with an offset of the differential amplifier A1 of, for example, 100 mV, the voltage drop across the sensor Ts will be about 100 mV. By means of the fed-back differential amplifier A1, the voltage at the terminal kl1 is stabilized. If the input I2 is connected via the reference voltage source V_{ref} to the supply line V_{SS}, with an offset of substantially 0V, the voltage at the terminal kl1 will be stabilized on substantially V_{ref}. The current measuring circuit CMS may be integrated with the integrated monolithic circuit, may be provided on a printed circuit board with the integrated monolithic circuit, may be incorporated in a testing apparatus for integrated monolithic circuits or may be present in an interface module on behalf of such a testing apparatus. In connection with the speed and with other testing methods "on-chip", such as, for example, "scan test", it is advantageous to integrate the current measuring circuit with the integrated monolithic circuit. The arrangement 1 further comprises signal processing means SPC for processing the quiescent current I_{DD}. The signal processing means SPC comprise the first transistor T1, which constitutes with the transistor Ts a current mirror configuration. Via an output electrode d1, a current is supplied, which is a mirror image of the quiescent current I_{DD}. Further, the arrangement 1 comprises comparison means COM for comparing the processed quiescent current I_O with a reference current I_{ref}. At an output 02 of the comparison means COM, an indication appears whether the reference current is exceeded by the current I_O. The indication may be digital; a logic "1" may then indicate, for example, exceeding.

Fig. 1B shows a current I_{DD} through an integrated monolithic digital circuit 2 as a function of the time t when supplying a given test vector at the inputs In thereof. t1, t2, t3 and t4 denote a few instants. At the instants t1 and t3, switching takes place in the integrated monolithic circuit 2. Between t1 and t2 and between t3 and t4, switching results in current peaks p1 and p2. Between t2 and t3 and after t4, the integrated monolithic digital circuit 2 is in the rest condition. In a CMOS circuit, for example a current peak has a value of the order of 10 mA and a quiescent current in a situation in which the CMOS circuit is not defective of the order of pA/nA. If there is a defect, such as, for example, a shortcircuit, the quiescent current may increase, for example, to an order of nA/mA. The measured current in the rest condition is I_O. If $I_O > I_{ref}$, this may indicate a defect in the CMOS circuit. The threshold value I_{ref} is adjustable.

It should be noted that the current measuring circuit can still be simplified by omitting the differential amplifier A1 and by then connecting the gate electrode gs to the terminal kl1, but due to low loop amplification a satisfactory stabilization of the voltage at the terminal kl1 is then not attained. It should further be noted that with different geometric dimensions of the transistors Ts and T1, current amplification can be obtained.

Fig. 2 shows an embodiment of signal processing means SPC and comparison means COM in an arrangement according to the invention. Symbols corresponding to Fig. 1A are indicated in the same manner. The signal processing means further comprise a differential amplifier A2, which is connected through a first input I3(+) to the first connection terminal kl1, through a second input I4(-) to the output electrode d1 of the first transistor T1 and through an output 03 to a gate electrode g2 of a second transistor T2. The transistor T2 is con-

nected by means of a first output electrode s2 to the output electrode d1 of the first transistor T1. A second output electrode d2 serv s to supply a current I_O to the comparison means COM. The comparison means COM comprise a current mirror configuration constituted by transistors T3 and T4 and having a first input I5 for supply of the processed quiescent current I_O, a second input I6 for supply of a reference current I_{ref} and a digital output 04. If the current I_O is smaller than I_{ref}, the output 04 assumes a first value ("O") and if $I_O > I_{ref}$, the output 04 assumes a second value ("O").

Fig. 3 shows a multiplication of a measured quiescent current. The signal processing means SPC comprise n transistors T1, ..., T1n and supply n output currents I_{01}, ..., I_{0n}. The transistors T1, ..., T1n may have increasing chip surfaces, as a result of which currents increasing in value may be obtained for further processing. The currents I_{01}, ..., I_{0n} may be supplied to analogue or digital comparison means. For I_{01} an analogous situation is shown; I_{01} is converted by a resistor R into a voltage U, which is supplied to an analogue voltage comparator (not shown), for example of the kind included in a testing apparatus for testing an integrated monolithic digital circuit.

Fig. 4A shows a current measurement according to the invention for measuring a metastable condition in a digital circuit. A metastable condition, i.e. an undefined output value "O" and "1", may occur, for example due to timing errors and occurs, for example, in flip-flops. A flip-flop as an integrated monolithic circuit 1 and an arrangement 2 according to the invention are shown. The flip-flop 1 has a data input D, a clock input C and an output Q. The arrangement 2 has control inputs S and an output 0. In a CMOS flip-flop, a comparatively high current (> 1mA) can be measured, which occurs due to a metastable condition. The output signal 0 can be used to delay the operation of circuits to be controlled by the flip-flop until the metastable condition has passed.

In Fig. 4B, I_{DD} is shown and in Fig. 4C U_Q, i.e. the voltage at the output Q of the flip-flop in a metastable condition is shown. It can be seen that a comparatively large current I_{DD} occurs during a metastable condition m. The normal starting situations for the flip-flops are indicated by "O" and "1".

In Fig. 5 a current measurement according to the invention is shown for obtaining information about the stability of outputs of combinatorial digital subcircuits. The arrangement 1 has additional inputs and outputs in the form of "handshake" signals H. The integrated monolithic digital circuit 2 has inputs I1, ..., In and outputs 01, ..., On. In the said circuits, it is difficult to detect when a stable condition is attained. By means of an arrangement according to the invention, an indication can be obtained whether an operation is carried out by the circuit 2. The quiescent curr nt arrangement 1 is then integrated with a so-called "handshake" system, which is required to couple such a circuit 2 to similar circuits. The arrangement 1 is set to the "ready for use" condition when a "handshake" signal is received and waits until a peak current has decreased to a quiescent current. The arrangement 1 then supplies a "handshake" signal to a similar circuit to indicate that data can be transferred. Delays are then no longer required between cascaded circuits, as a result of which in principle circuits operating at a higher speed can be obtained.

Fig. 6 shows a testing apparatus TD provided with an arrangement 1 according to the invention. The arrangement 1 may also be constructed as an interface for a testing apparatus TD. An apparatus commercially available for testing VLSI circuits is, for example, a "Sentry 50" tester of Schlumberger. The arrangement according to the invention can be entirely or partly incorporated therein.

Fig. 7A shows an embodiment of the current measuring circuit CMS with an embodiment of the modification circuit M. The operational amplifier A1 (see Fig. 1A) is constituted by the transistors T5, T6, T7, T8, T9 and T10 and the modification circuit is constituted by the transistor TM. The remaining reference symbols correspond to those in Fig. 1. In the embodiment shown, the stability is also guaranteed outside the quiescent current measurement when considerably larger currents flow because in the configuration chosen A1 then has a low amplification.

Fig. 7B shows another embodiment of the modification circuit M, which is coupled to the output 01 of the amplifier A1 in Fig. 1 and to the input gs of the current sensor Ts. The modification circuit M comprises an inverter T11, T12 coupled to the transistor TM. A clock signal CI is supplied to an input I_3 of the inverter from, for example, the clock generator of the circuit 2, the "Device Under Test" (DUT). Since the inverter has a fixed delay, the phase of the clock signal should be such that the modification circuit M switches more rapidly than the DUT.

Figs. 8A and 8B show configurations of integrated circuits (IC's) including a current measuring arrangement according to the invention. The IC has besides the pins usually present an additional Pe in the configuration shown in Fig. 8A. If the IC includes circuits drawing large currents, which remain outside the I_{DDQ} measurement, because of the fact that the circuits drawing large currents are already supplied via an additional pin, i.e. the additional pin for I_{DDQ} measurement, the terminal kl1 is then floating and V_{DD} is supplied to kl2. Fig. 8B

shows such a configuration.

Fig. 9 shows the coupling of the current measuring arrangement according to the invention with a scan chain in an IC. A scan chain, which is well known, is constituted by a number of flip-flops ..., FFn-1, FFn in an IC during testing of the IC. The flip-flops in the IC are joined to form a shift register by means of multiplexers ..., Mn-1, Mn during testing. Data are supplied to a multiplexer at the beginning of a scan chain at an input SI and are clocked in into the shift register thus formed. At the end of the scan chain, test data become available again at an output SO at an IC pin. An I_{DDQ} monitor MON according to the invention can be coupled to the scan chain, for example via an additional multiplexer, at a predetermined point in the scan chain. The scan chain is switched on by a control signal Tst. Since a pin was already necessary for the scan test, no additional pin is required for the I_{DDQ} measurement. The I_{DDQ} monitor MON can also be multiplexed with the output of the scan chain. In the scan test mode, that is to say that the signal Tst has a first value, the output of the scan chain is passed to an IC pin, while in the normal mode, that is to say that the signal Tst has a second value, the output of the I_{DDQ} monitor is passed to the IC pin. Per IC, several I_{DDQ} monitors can be present, which can all be coupled to the scan chain.

For testing printed circuit boards (PCB's), an integrated circuit can be formed comprising an I_{DDQ} monitor according to the invention and a so-called boundary scan controller, which is well known per se. The I_{DDQ} monitor then measures the current through a supply line, which is connected to a number of IC's to be measured. The result of the current measurement can then be stored in a register in the boundary scan controller.

Fig. 10 shows the coupling of the current measuring arrangement MON according to the invention with a self-test circuit ST in an integrated circuit IC. The monitor MON measures the quiescent current I_{DDQ} of the logic circuit LC. The self-test circuit ST is connected not only to outputs 01, 02, ... On of the logic circuit LC, but also to the output OM of the monitor. If a self-test circuit is present in the IC, in this manner no additional pin for the I_{DDQ} monitor is required. The self-test circuit is, for example, a so-called "linear feedback shift register", which is well known in the field of testing.

It should be noted that the number of applications is not limited to the applications described. For example, when providing (parts of) the arrangement (in multiple) on a printed circuit board, the current measurement may be used for "connectivity checking", i.e. detecting interrupted print tracks or shortcircuits between print tracks. The arrangement according to the invention may also be included in a "boundary scan chain". Besides in MOS technique, the arrangement may also be constructed in another technique, such as, for example, a bipolar technique.

It should further be noted that with integration of the I_{DDQ} monitor in an IC having circuits whose I_{DDQ} is measured, the I_{DDQ} monitor typically occupies about 1% of the "active area". In such a case, the monitor is arranged at an unused area at the periphery of the IC. In general no additional processing steps are required for also integrating the I_{DDQ} monitor.

Claims

1. An arrangement for measuring a quiescent current of an integrated monolithic digital circuit, which arrangement comprises a transistor as current sensor for measuring the quiescent current, which is provided with a first connection terminal for coupling to a supply terminal of the integrated monolithic circuit and with a second connection terminal for coupling to a supply, characterized in that the arrangement comprises voltage stabilization means for stabilizing a voltage at the first connection terminal and signal processing means coupled to the voltage stabilization means for signal processing of the quiescent current.

2. An arrangement as claimed in Claim 1, characterized in that the voltage stabilization means comprise a differential amplifier, of which a first input is coupled to the first input terminal, a second input is coupled to the second connection terminal or to a connection terminal for connection to a reference voltage source and an output is coupled to a gate electrode of a transistor.

3. An arrangement as claimed in Claim 1 or 2, characterized in that the output of the differential amplifier is coupled to the gate electrode via a modification circuit for modifying the operation of the current sensor outside a quiescent current measuring period or outside a quiescent current measurement of the integrated monolithic circuit.

4. An arrangement as claimed in Claim 3, characterized in that the modification means that the current sensor in the form of a transistor is made fully conducting.

5. An arrangement as claimed in Claim 1, 2, 3 or 4, characterized in that the signal processing means comprise a first transistor, which constitutes with the current sensor in the form of a transistor a current mirror configuration, which is designed to supply via an output electrode of the first transistor a current, which is a current imag of the quiescent current.

6. An arrangement as claimed in Claim 5, characterized in that the signal processing means comprise a differential amplifier, which is coupled

through a first input to the first input terminal, through a second input to the output electrode of the first transistor and through an output to a gate electrode of a second transistor, which second transistor is coupled through a first output electrode to the output electrode of the first transistor, while a second output electrode of this second transistor serves to supply a further processed quiescent current.

7. An arrangement as claimed in Claim 5 or 6, characterized in that the signal processing means comprise further transistors, which constitute with the current sensor a current mirror configuration, while for obtaining the different processed quiescent currents the transistors of the signal processing means have different geometric dimensions.

8. An arrangement as claimed in any one of the preceding Claims, characterized in that the arrangement comprises comparison means coupled to the signal processing means for comparing the processed quiescent current with at least one reference current or reference voltage, the comparison means being designed to indicate when the reference current or reference voltage is exceeded.

9. An arrangement as claimed in Claim 8, characterized in that the comparison means comprise at least one current mirror configuration having a first input for the supply of a processed quiescent current, a second input for the supply of a reference voltage and a digital output assuming in dependence upon the processed quiescent currents with respect to the reference currents a first and a second value, respectively.

10. An arrangement as claimed in Claim 8, characterized in that the comparison means are constituted by analogue voltage comparison means.

11. An arrangement as claimed in Claim 8, 9 or 10, characterized in that an output of the comparison means is coupled to a scan chain.

12. An arrangement as claimed in Claim 8, 9 or 10, characterized in that the output of the comparison means is coupled to a self-test circuit.

13. An integrated monolithic digital circuit comprising at least one subcircuit, characterized in that the integrated monolithic circuit comprises at least one arrangement or at least a part thereof as claimed in any one of the preceding Claims for measuring the quiescent current of subcircuits, of combinations of subcircuits or of all subcircuits.

14. An integrated monolithic digital circuit comprising an arrangement as claimed in any one of Claims 1 to 10 and a boundary scan logic circuit for testing integrated circuits on printed circuit boards, in which the quiescent current measuring arrangement and the boundary scan logic circuit are coupled to ach other.

15. A testing apparatus for measuring a quiescent current of an integrated monolithic digital circuit, characterized in that the testing apparatus comprises at least a part of the arrangement as claimed in any one of Claims 1 to 10.

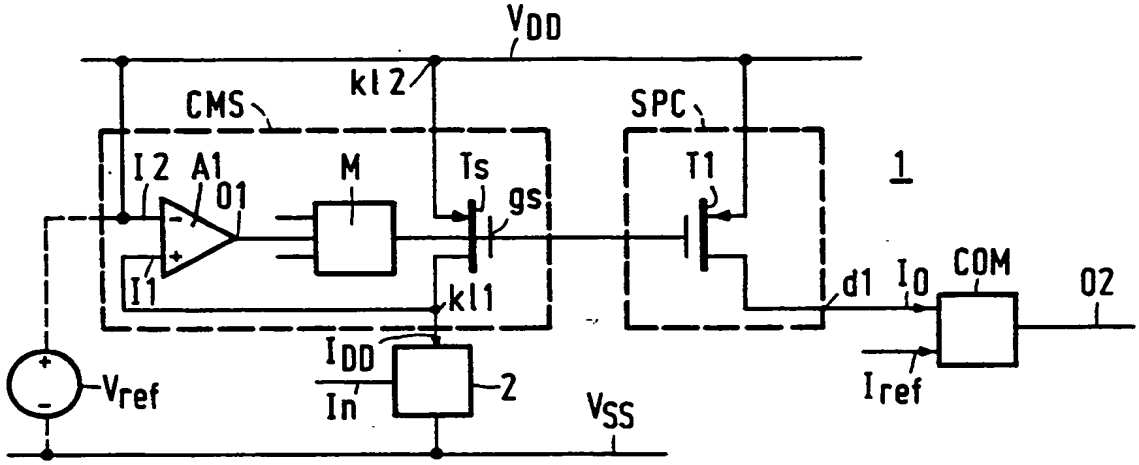

FIG.1A

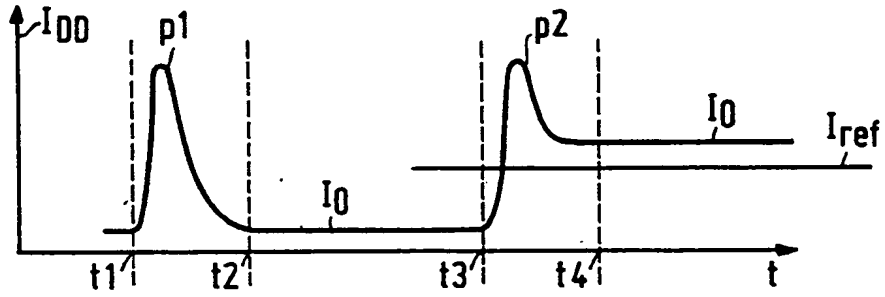

FIG.1B

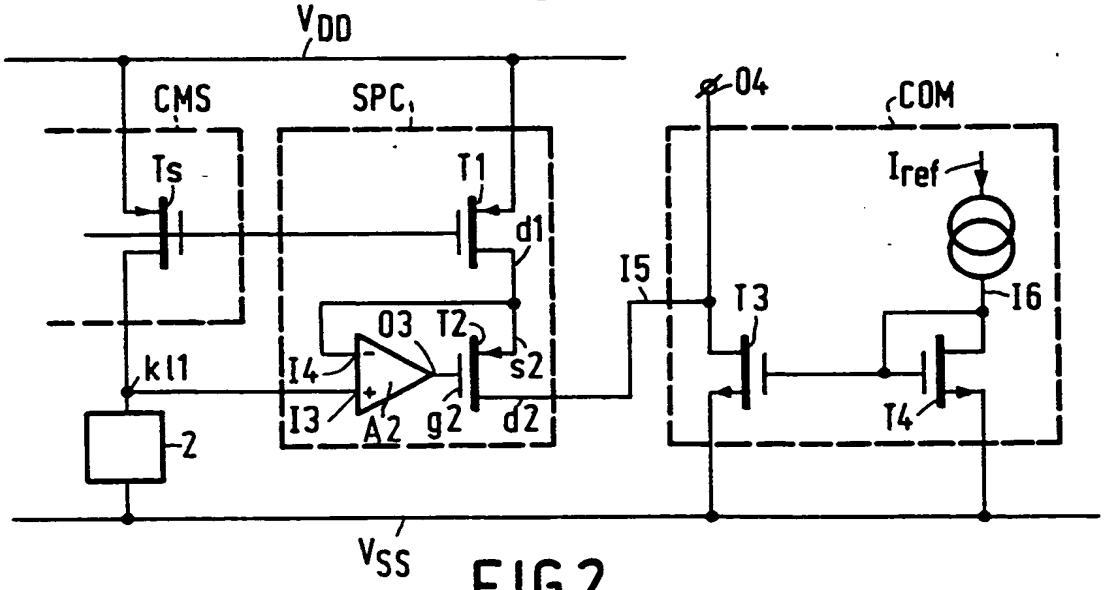

FIG.2

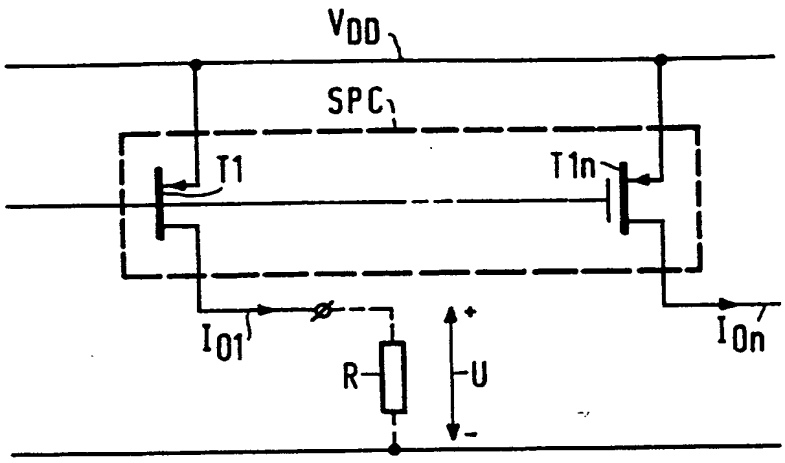

FIG.3

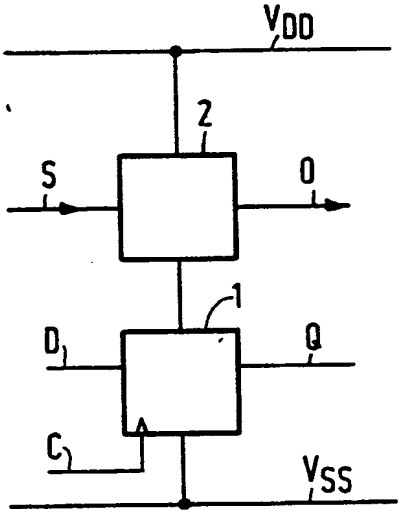

FIG.4A

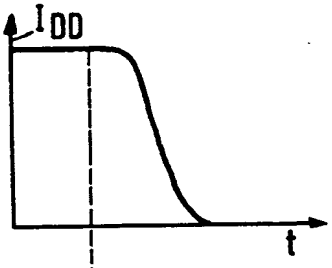

FIG.4B

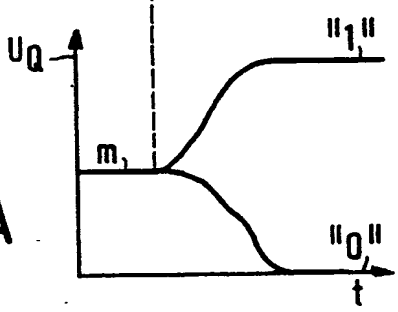

FIG.4C

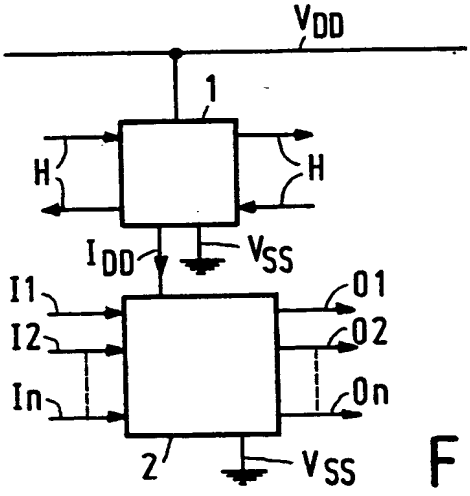

FIG.5

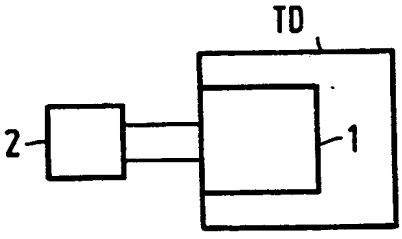

FIG.6

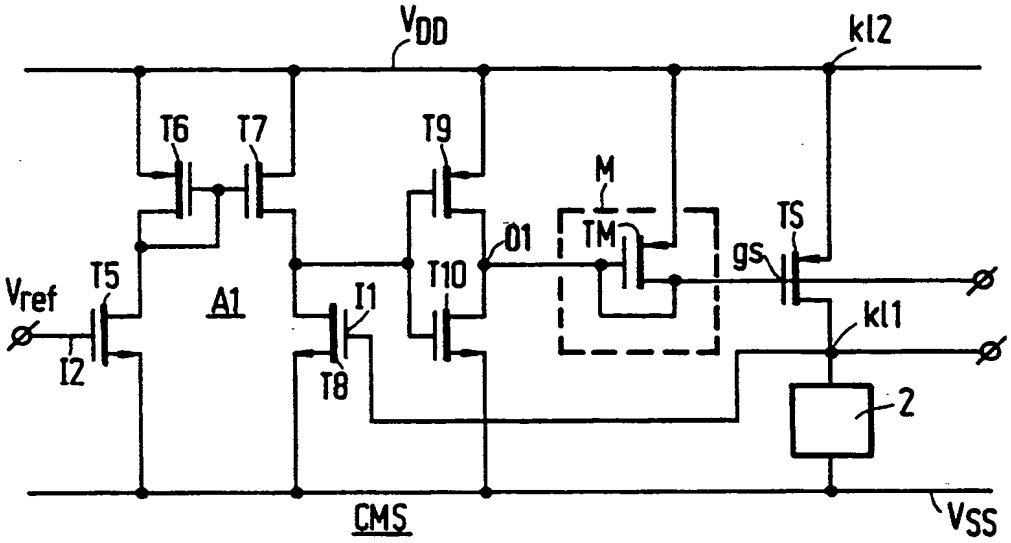

FIG. 7A

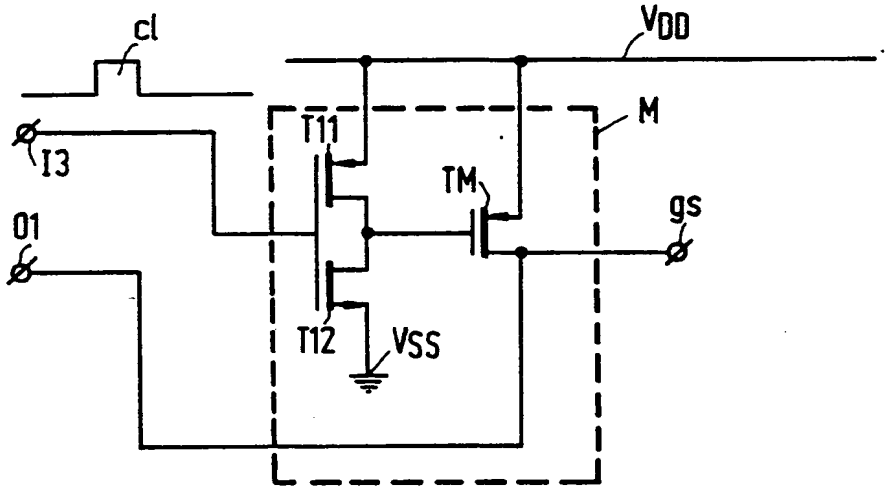

FIG. 7B

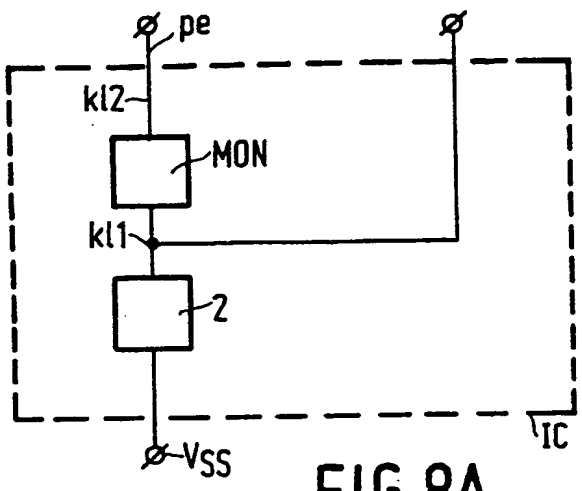

FIG.8A

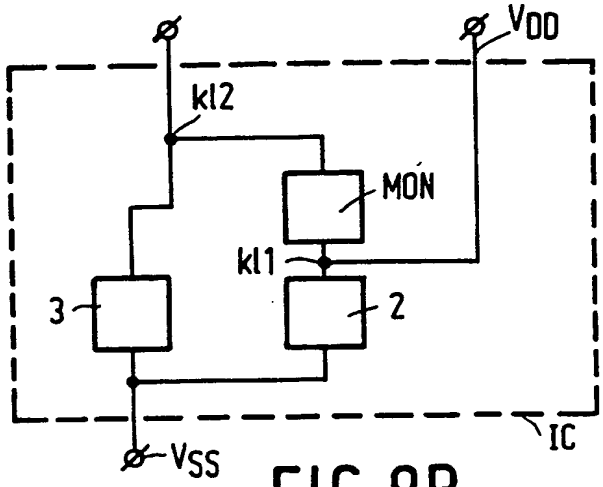

FIG.8B

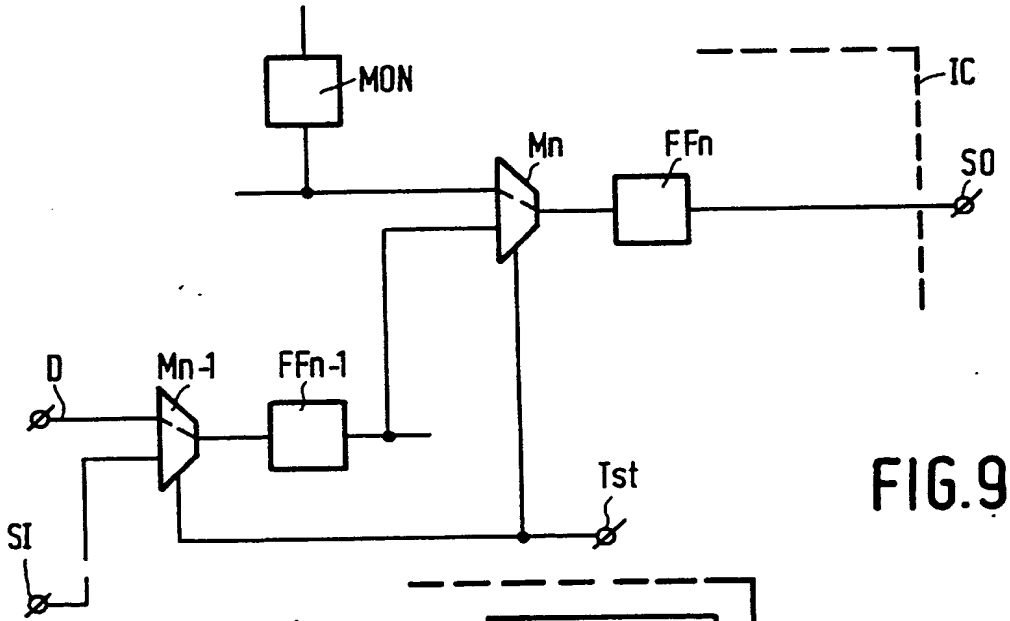

FIG.9

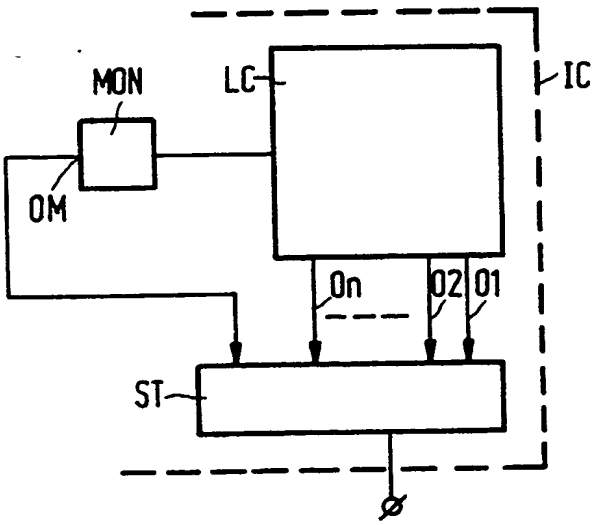

FIG.10

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(54) Arrangement for measuring a quiescent current of an integrated monolithic digital circuit, integrated monolithic digital circuit provided with such an arrangement and testing apparatus provided with such an arrangement.

(57) An arrangement is proposed for measuring a quiescent current of a digital IC. The arrangement comprises a current sensor in series with the IC and the supply, voltage stabilization means for stabilizing the voltage across the IC and signal processing means coupled thereto for processing the measured quiescent current. The quiescent current is measured when no flip-flops are switched in the IC. By means of the arrangement, there can be measured rapidly and accurately whether the quiescent current assumes an abnormal value, which indicates that the IC exhibits defects. The signal processing means comprise a current mirror, which is coupled to a current comparator circuit supplying a digital output signal for determining a defect.

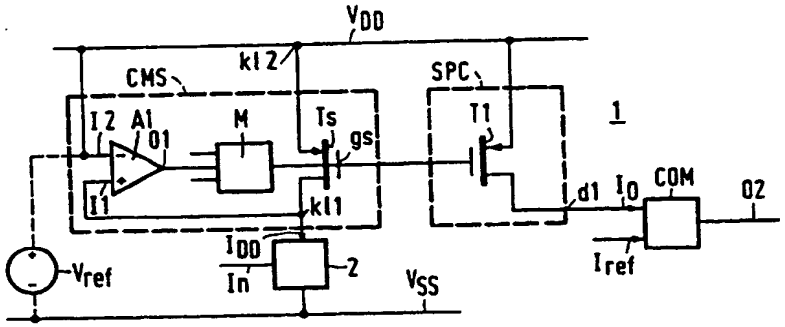

FIG.1A

EP 0 386 804 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 20 0016

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
Y	IEEE 1987 INTERNATIONAL TEST CONFERENCE PROCEEDINGS, Washington D.C., 1st - 3rd September 1987, paper 13.1, pages 300-309, IEEE Computer Society Press, New York, US; L.K. HORNING et al.: "Measurements of quiescent power supply current for CMOS ICs in production testing" * Page 302, column 1, paragraph 3 - page 303, column 1, line 24; page 306, column 2, lines 10-52 *	1,2,5-10,15	G 01 R 31/28 G 01 R 19/15
A	IDEM	3,4,8	
Y	EP-A-0 227 149 (N.V. PHILIP'S GLOEILAMPENFABRIEKEN) * Column 3, line 45 - column 7, line 51; fig. *	1,2,5-10,15	
A	EP-A-0 274 995 (SGS MICROELETTRONICA S.p.A.) * Column 2, line 34 - column 3, line 19; column 3, line 53 - column 4, line 1; fig. *	13	TECHNICAL FIELDS SEARCHED (Int. Cl.5) G 01 R
A	PATENT ABSTRACTS OF JAPAN, vol. 7, no. 198 (P-220)[1343], 2nd September 1983; & JP-A-58 96 259 (MITSUBISHI DENKI K.K.) 08-06-1983	13	
A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 1A, June 1984, pages 240-244, New York, US; Y.H. CHAN et al.: "Variable standby current source scheme" * Page 241, paragraph 1 *	13,15	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	02-08-1990	HOORNAERT W.

CATEGORY OF CITED DOCUMENTS

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